1. (Amended) A ball grid array package semiconductor device, the device being supplied with two or more external powers including a first power and a second power, the device comprising:

a semiconductor chip having a plurality of pads arranged along a first surface thereof;

a substrate having a first surface which confronts the first surface of the semiconductor chip and an opposite second surface, the substrate further having a slot extending there through which is aligned over the plurality of pads to expose the plurality of pads;

a bonding material inserted between the respective first surfaces of the semiconductor chip and the substrate to fix the semiconductor chip to the substrate;

a first signal line plane extending over a first two-dimensional area of the second surface of the substrate on one side of the slot;

a second signal line plane extending over a second two-dimensional area of the substrate;

a first plurality ball mounts located within the first two-dimensional area of the first signal line plane;

a second plurality of ball mounts located within the second two-dimensional area of the second signal line plane;

a first plurality of balls respectively mounted within the first plurality of ball mounts, wherein some of the first plurality of balls are electrical connected to the first signal line plane and others of the first plurality of balls are electrically isolated from the first signal line plane;

a second plurality of balls respectively mounted within the second plurality of ball mounts, wherein some of the second plurality of balls are electrical connected to the second signal line plane and others of the second plurality of balls are electrically isolated from the second signal line plane; and

a plurality of wirings for connecting the first and second signal planes and at least some of the first and second plurality of balls to respective pads of the semiconductor chip through the slot;

wherein the first power is applied to at least one of the first plurality of balls which is electrically to the first signal line plane, and wherein the second power is applied to at least one of the second plurality of balls which is connected to the second signal line plane.

11. (Amended) A ball grid array package semiconductor device having a plurality of balls, including a plurality of power balls and a plurality of ground balls, the ball grid array package semiconductor device comprising:

a semiconductor chip comprising a plurality of pads, including a plurality of power pads and a plurality of ground pads, arranged along a first surface thereof; and

a single layer substrate having a first surface which confronts the first surface of the semiconductor chip and an opposite second surface, the substrate further including a slot extending there through which is aligned over the plurality of pads to expose the plurality of pads;

a power plane extending over a first two-dimensional area of the second surface of the substrate on one side of the slot, the power plane including power ball mounts, power balls and the power pads;

a ground plane extending over a second two-dimensional area of the second surface of the substrate on one side of the slot, the ground plane including ground ball mounts, ground balls and the ground pads; and

a plurality of signal ball mounts located within and electrically isolated from at least one of the first and second two-dimensional areas of the power plane and the ground plane, respectively;

wherein the semiconductor chip is mounted to the first side of the substrate such that the plurality of pads are electrically connected to the power ball mounts, the ground ball mounts and the signal ball mounts.

ATTACHMENT "A"

1. (Amended) A ball grid array package semiconductor device, the device being supplied with two or more external powers including a first power and a second power, the device comprising:

a semiconductor chip having a plurality of pads arranged along [~~a center of~~] a first surface thereof;

a substrate having a first surface which confronts the first surface of the semiconductor chip and an opposite second surface, the substrate further having a slot extending there through which is aligned over [~~of a predetermined size and centrally arranged in a spaced relationship to~~] the plurality of pads to expose the plurality of pads[~~, the substrate having a signal line plane including a signal line pattern and a plurality of ball mounts on its one side, and wherein the semiconductor chip is mounted on an other side thereof~~];

a bonding material inserted between the respective first surfaces of the semiconductor chip and the substrate to fix the semiconductor chip to the substrate; [~~and~~]

a first signal line plane extending over a first two-dimensional area of the second surface of the substrate on one side of the slot;

a second signal line plane extending over a second two-dimensional area of the substrate;

a first plurality ball mounts located within the first two-dimensional area of the first signal line plane;

a second plurality of ball mounts located within the second two-dimensional area of the second signal line plane;

a first plurality of balls respectively mounted within the first plurality of ball mounts, wherein some of the first plurality of balls are electrical connected to the first signal line plane and others of the first plurality of balls are electrically isolated from the first signal line plane;

a second plurality of balls respectively mounted within the second plurality of ball mounts, wherein some of the second plurality of balls are electrical connected to the second signal line plane and others of the second plurality of balls are electrically isolated from the second signal line plane; and

a plurality of wirings for connecting the first and second signal planes and at least some of the first and second plurality of balls to respective pads of the semiconductor chip through the slot;

wherein the first power is applied to at least one of the first plurality of balls which is electrically to the first signal line plane, and wherein the second power is applied to at least one of the second plurality of balls which is connected to the second signal line plane

[~~a plurality of balls mounted on the plurality of ball mounts to be connected to an external circuit,~~

~~wherein the signal line plane is divided into two or more signal line planes including a first line plane and a second line plane, and~~

~~wherein lines for the first power are formed only on the first signal line plane, and lines for the second power are formed only on the second signal line plane~~].

11. A ball grid array package semiconductor device having a plurality of balls, including a plurality of power balls and a plurality of ground balls, the ball grid array package semiconductor device comprising:

a semiconductor chip comprising a plurality of pads, including a plurality of power pads and a plurality of ground pads, arranged along a [center of a] first surface thereof; and

a single layer substrate having a first surface which confronts the first surface of the semiconductor chip and an opposite second surface, the substrate further including a slot extending there through which is aligned over [~~of a predetermined size centrally arranged in a spaced relationship to~~] the plurality of pads to expose the plurality of pads[, and, on one side thereof having];

a power plane extending over a first two-dimensional area of the second surface of the substrate on one side of the slot [~~,on a first portion of a surface of the one side around the slot~~], the power plane including power ball mounts, power balls and the power pads;

a ground plane extending over a second two-dimensional area of the second surface of the substrate on one side of the slot [~~on a second portion of the surface of the one side around the slot~~], the ground plane including ground ball mounts, ground balls and the ground pads; and

a plurality of signal ball mounts located within and electrically isolated from at least one of the first and second two-dimensional areas of the power plane and the ground plane, respectively[,];

wherein the semiconductor chip is mounted [~~on an other~~] to the first side of the substrate such that the plurality of pads are electrically connected to the power ball mounts, the ground ball mounts and the signal ball mounts.